REMARKS

Claims 28-29, 33, 35 and 37-39 are pending in the present application. With entry of this Amendment, Applicant amends claim 28. Reexamination and reconsideration are respectfully requested.

The Examiner rejected claims 28-29, 33, 35 and 37-39 under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art figure 1 in view of U.S. Patent No. 6,333,672 (Baskett). The rejection is respectfully traversed for each claim as set forth below.

Claim 28

The Examiner contends that the "admitted prior art includes all of the limitations" of claim 28 "except for the limitation of the cascade transistors and trickle current sources (the recited second and third current sources)." (Office Action, December 29, 2005 at 2.) In light of the amendment to claim 28, it is respectfully submitted that the rejection has been overcome.

Independent claim 28 has been amended to recite, in part:

> A digital to analog converter comprising:
> a first analog current summing bus having one end coupled to ground;
> a second analog current summing bus having one end coupled to ground; and
> a plurality of current switches, each switch including:
>
> . . .
>
> a pair of cascode transistors having emitters respectively coupled to the collectors of said differential pair of transistors, and collectors coupled to the other ends said first and second current summing buses, respectively; and . . .

The amendment to claim 28 clearly specifies the coupling of a plurality of the collectors of the cascode transistors to their respective analog current summing buses which are connected to ground. This is different from the cascode transistors in Fig. 1 of Baskett which shows the

collectors of the single pair of cascode transistors coupled to a single digital output circuit which is connected to V_{cc}. Hence, there is no motivation to combine Baskett with the admitted prior art.

Applicants note that, even though the Supreme Court noted in *KSR International Co. v. Teleflex, Inc.*, No. 04-1350, at * 17 (2007), that prior art teachings need not be precise teachings directed to the specific subject matter, the Court nevertheless warned against "hindsight bias and . . . arguments reliant upon *ex post* reasoning." Here, in order to achieve the present invention, a person skilled in the art must not only have the motivation to combine admitted prior art figure 1 and Baskett, she must also take a further step to modify Baskett. While currently, in hindsight, it may seem convenient to modify Baskett to achieve the present invention, it would not have been obvious to one skilled in the art at the time of the invention. As noted in the Rule 132 declaration of Don Devendorf, one of the inventors, one skilled in the art at the time of the invention would not have attempted to combine a digital circuitry (logic gate), taught in Baskett, with an analog circuit (digital to analog converter), as taught in the admitted prior art, because it was not common digital to analog converter design practice to do so. (Rule 132 Declaration of Don Devendorf ("Devendorf Decl."), Ex. A ¶ 2.) For example, because the present invention contains multiple digital to analog (DAC) cells (as compared to Baskett which only has one), the multiple outputs of each DAC cell must be summed together into one load resister to create the analog output of the overall digital to analog converter circuitry. A person skilled in the art would not even consider using Baskett because the output of Baskett is digital (and only has the binary state of zero or one) rather than the analog output required in the present invention.

As previously noted, unlike Baskett, which only has one current switch, the present invention combines a plurality of current switches in a summing bus to achieve the analog output. Each current switch contains a separate cascode/trickle current circuit for better matching. This serves a novel purpose in the present invention in that it reduces the analog output signal level dependent nonlinear switching time modulation, meaning that from one digital input to the next, the output will settle in the same time period instead of varying depending on the analog output signal level. By providing such a consistent switching time, the spur free dynamic range of the digital to analog converter is greatly improved. In contrast, small variations in switching time do not affect

the digital output of Baskett since the output in Baskett is a digital state, not an analog level. In fact, the digital output of Baskett is not affected by any analog signal dependent switching time variations. Hence, digital logic gates (such as in Baskett) do not benefit from such improvement (reduction) in analog output signal level dependent nonlinear switching time modulation.

In addition, the Court in *KSR International* reaffirmed the need to consider the secondary considerations (*e.g.*, long felt but unsolved needs, commercial success, etc.) noted in *Graham v. John Deere Co. of Kansas City*, 383 U. S. 1 (1966) in determining indicia of nonobviousness. *KSR Int'l*, at *2. It is important to note that, while cascade transistors are known to a person skilled in the art at the time of the invention, as shown in Baskett, the addition of cascade transistors to a digital to analog converter to solve analog distortion and improve performance is novel and nonobvious. Here, as noted by Don Devendorf, the present invention is achieved only after months of experiments and tests on actual builds of prototypes because computer simulation could not provide accurate real world results. (Devendorf Decl., Ex. A, ¶ 2.) During these tests, the inventors had to experiment with different architectures, process technologies and devices to achieve the present invention. (*Id.*) Moreover, the invention also solved the long felt but unsolved need in the industry by providing superior isolation leading to significant reduction of the analog output spurious signals. (*Id.*) This has led to the successful commercialization of the present invention. (*Id.*) These secondary indicia of nonobviousness further show that the present invention is novel.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If, for any reason, the Examiner finds the application other than in condition for allowance, Applicants request that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5587 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any

required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 535352003600.

Dated: August 31, 2007

Respectfully submitted,

By Alex Yap

Alex S. Yap
Registration No.: 60,609
MORRISON & FOERSTER LLP
555 West Fifth Street, Suite 3500
Los Angeles, California 90013
(213) 892-5200